ESSENTIALS FOR ESD PROGRAMS & EOS/ESD SYMPOSIUM FOR FACTORY ISSUES

Essentials for ESD Programs Seminar & EOS/ESD Symposium for Factory Issues November 5-8, 2012 TÜV SÜD PSB Pte. Ltd., 1 Science Park Drive, SINGAPORE, 118221

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ESSENTIALS FOR ESD PROGRAMS & EOS/ESD SYMPOSIUM FOR FACTORY ISSUES

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SCHEDULE

MONDAY-TUESDAY, NOVEMBER 5-6, 2012

8:00 AM - 5:00 PM
Seminar: Essentials for ESD Programs - Factory Technologies • Controls • Procedures

WEDNESDAY, NOVEMBER 7, 2012

9:00 AM - 10:00 AM	10:00 AM - 10:30 AM	10:30 AM - 12:10 PM	12:10 PM - 1:30 PM	1:30 PM - 2:45 PM	2:45 PM - 3:15 PM	3:15 PM - 4:30 PM	4:30 PM - 5:00 PM	5:00 PM - 6:00 PM	6:00 PM - 7:00 PM
Invited Talk 1:	Break Exhibits Open	Technical Session 1A	Lunch Exhibits Open	Technical Session 1B	Break Exhibits Open	Technical Session 1C	Break Exhibits Open	Workshop	Reception

THURSDAY, NOVEMBER 8, 2012

9:00 AM - 10:00 AM	10:00 AM - 10:30 AM	10:30 AM - 12:10 PM	12:10 PM - 1:30 PM	1:30 PM - 2:45 PM	2:45 PM - 3:15 PM	3:15 PM - 4:55 PM	4:55 PM - 5:30 PM
Invited Talk 2	Break Exhibits Open	Technical Session 2A	Lunch Exhibits Open	Technical Session 2B	Break Exhibits Open	Technical Session 2C	Break Exhibits Open

MONDAY-TUESDAY, NOVEMBER 5-6, 2012

8:00 AM - 5:00 PM Seminar: Essentials for ESD Programs Factory: Technologies • Controls • Procedures

WEDNESDAY, NOVEMBER 7, 2012

9:00 AM - 10:00 AM Invited Talk 1: ESD Basics; Reinhold Gaertner
10:00 AM - 10:30 AM Break-Exhibits Open
10:30 AM - 12:10 PM Technical Session 1A
- 1A.1: Issues & Solutions Involving Tape & Reel Induced ESD
- 1A.2: Humidity Control Device for Static Charge Reduction
- 1A.3: S20.20 ESD Improvements for the Factory Floor
- 1A.4: "Volume Conductive" Polyurethane and Epoxy Sealings and Thick Coatings Meet the Latest ESD Standards

12:10 PM - 1:30 PM Lunch-Exhibits Open
1:30 PM - 2:45 PM Technical Session 1B
- 1B.1: EOS Risk to Thin Oxides Contributed by Wrist-Strap Monitors
- 1B.2: CDM Risk Mitigation with Air Ionization in Hi-Temp Automated Test Handler
- 1B.3: Process ESD Compatibility Measurements

2:45 PM - 3:15 PM Break-Exhibits Open
3:15 PM - 4:30 PM Technical Session 1C
- 1C.1: Experiences with an Alternative Method for Grounding Personnel During Sitting Operation
- 1C.2: A Comparison of Electrostatic Discharge Models and Failure Signatures for Light-Emitting Diode
- 1C.3: Implementing Air Ionizing Blower at KLA Tencor 2401 Metrology Tool Reduce Visual Inspection Failure for Semiconductor Wafers

4:30 PM - 5:00 PM Break-Exhibits Open
5:00 PM - 6:00 PM Workshop
6:00 PM - 7:00 PM Reception

THURSDAY, NOVEMBER 8, 2012

9:00 AM - 10:00 AM Invited Talk 2: S20.20 Program Development; John Kinnear
10:00 AM - 10:30 AM Break-Exhibits Open
10:30 AM - 12:10 PM Technical Session 2A
- 2A.1: Investigating The Performance of Vacuum Formed Conductive and Dissipative Trays Which are used for Handling and Storage of ESDs
- 2A.2: ESD Levels and Trends for Advanced Memory Technologies
- 2A.3: Novel Strap to Achieve Less than 50 Volt HBM on Normal Footwear
- 2A.4: Comparing Room Ionization Technologies in FPD Manufacturing

12:10 PM - 1:30 PM Lunch-Exhibits Open
1:30 PM - 2:45 PM Technical Session 2B
- 2B.1: Reduction of Coupled Voltage of Electric Cable with Electro-Static Countermeasure
- 2B.2: Compliance Verification of Static Dissipative Carrier for ESDS Devices in Semiconductor Backend Testing
- 2B.3: Evaluation of the Performance of Corona and Hybrid Alpha Ionizer Technology in Air and Nitrogen

2:45 PM - 3:15 PM Break-Exhibits Open
3:15 PM - 4:55 PM Technical Session 2C
- 2C.1: EMI-Caused EOS Exposure of Components and its Mitigation
- 2C.2: HBM Concerns on Semiconductor Component (ICs) Mounted in Frame Form During Backend Manufacturing Processes
- 2C.3: ESD Control at Tape Drive and Tape Head Manufacturing
- 2C.4: Minimizing Electrostatic Charge Generation and ESD Event in TFT-LCD Production Equipment

4:55 PM - 5:30 PM Break-Exhibits Open

SEMINAR

Essentials for ESD Programs

FACTORY: TECHNOLOGIES • CONTROLS • PROCEDURES

NOV. 5-6, 2012 • 8:00 A.M. - 5:00 P.M.

Instructors: John Kinnear, *IBM*; Yong Hoon (Joshua) Yoo, *Core Insight, Inc.*

This two-day seminar consists of concentrated versions of the ten ESDA tutorials which comprise the ESDA Program Manager (PrM) Certification Program:

- ESD Basics for the Program Manager
- Ionization and Answers for the Program Manager
- Packaging Principles for the Program Manager
- System Level ESD/EMI: Testing to IEC and Other Standards
- Cleanroom Considerations for the Program Manager
- How To's of In-Plant ESD Survey and Evaluation Measurements
- Device Technology and Failure Analysis Overview
- Electrostatic Calculations for the Program Manager and the ESD Engineer
- ESD Standards Overview for the Program Manager
- ESD Program Development & Assessment (ANSI/ESD S20.20 Seminar)

Key concepts and information from the above courses have been selected for this two-day seminar. Many of the demonstrations and videos from ESD Basics Tutorial are included in this seminar. Examples of electrostatics and ESD calculations are included where appropriate throughout the seminar.

*This Seminar offers a broad exposure to the essentials of ESD programs. It offers a two-day comprehensive set of factory technologies and procedures designed for managers, technicians, and specialists desiring ESD control program training and information. This course serves as a refresher class to those taking the PrM Certification exam. In addition, the course can be used as part of the preparation for those interested in taking the iNARTE Engineering or Technician Certification exam, which will be offered on the day following this two-day course.

DAY 1

PART I (8:00 A.M.-12:00 P.M.)

This section reviews the fundamentals of electrostatics, charge flow, electric field and voltage. The concept of capacitance and the fundamental relationship, Q = CV, is introduced and explored with demonstrations and videos. The practical application of these concepts to the measurement of resistance, fields and voltages, and the relevant standards are reviewed and demonstrated.

PART II (1:00 P.M.-5:00 P.M.)

The principles from Part I are then applied to grounding principles and standards, measurement of charge, standard models for ESD (i.e., human-body model and charged device model), and static induction with demonstrations and videos. Very simple and basic ESD protection circuit concepts and relevant failure analysis techniques are introduced and reviewed.

DAY 2

PART III (8:00 A.M.-12:00 P.M.)

Key ESD technical areas are reviewed such as air ionization, ESD-safe packaging, cleanroom principles and electrostatic attraction. Standards relevant to these areas are described.

PART IV (1:00 P.M.-5:00 P.M.)

The final section includes charge generation test methods, additional ESDA standards, system-level ESD standards and testing, practical auditing techniques and strategies, and ESD event detection. The tutorial concludes with a review of ESD Protected-Areas (EPAs), ESD Program Management and the application of ANSI/ESD S20.20.

ABOUT THE INSTRUCTORS

John Kinnear is an IBM Senior Engineer specializing in process & system technology, and facility certification in accordance with ANSI/ESD S20.20. He has a BS degree from University of Buffalo and a MS degree from Syracuse University. John has coordinated the testing of large mainframes for compliance to EMC, Safety, Environmental, Shipping and Volatile Organic Emission standards. He has also been the lead engineer on testing large mainframe systems to EMC emissions and immunity standards for FCC, CE Mark, VCCI and other national requirements. As a member of the ESD Association since 1990, John has served in several Standards Development Committees as well as association management positions. John is the appointed Technical Adviser to the United States National Committee/IEC Technical Committee 101, where he represents the United States to the International Electrotechnical Commission (IEC). As Chair of the ESDA's Facility Certification (ANSI/ESD S20.20) development program, John played major roles in the program's development and industry launch. In particular, John coordinated the initial development of Lead Assessor training, ISO Registrar Certification, and witness audits. John has served in every ESD Association officer's position, including Vice President, Senior Vice President and President. He is the past Chairman of the EOS/ESD Symposium Technical Program Committee and past General Chairman of the 2004 EOS/ESD Symposium.

Yong Hoon (Joshua) Yoo has been involved in the static control industry since 1994 and started his own company, CORE INSIGHT, INC. for advanced static control products and services based in Korea. He has experience with micro contaminations control and invented alternative ionization technology for FPD industry. Joshua earned a degree in business administration and information & communication engineering from Hanyang University. He is an active member of the SEMI ESD Taskforce and is an iNARTE certified ESD Engineer as well as an ESD Association Certified Professional ESD Program Manager. Joshua has been a member of ESD Association since 2000 and is founder and president of the Korea Chapter of the ESD Association. He is currently an editorial advisor to the ESD Association newsletter Threshold.

INVITED TALKS

WEDNESDAY, NOVEMBER 7, 2012

Invited Talk 1: ESD Basics

Reinhold Gaertner, Infineon Technologies

This talk will discuss the Fundamental causes of ESD and its control. It includes how ESD impacts industry, with brief explanations of charge generation, field measurement, the role of capacitance and voltage, charge measurement, and charge decay. Device failure mechanisms, including the respective test models like Human Body Model or Charged Device Model, will also be explained. Reinhold will discuss how to protect ESD sensitive devices and assemblies, give definitions of an Electrostatic Protected Area (EPA), and show how to assess the risk in an automated production line.

Reinhold Gaertner received his diploma in physics from the Technical University of Munich in 1987. Then he joined the University of the Federal Armed Forces in Munich, working on measurement techniques for ESD protective packing materials. After working as an independent ESD consultant he joined Siemens Semiconductors in 1996 which is now Infineon Technologies. As senior principal engineer he has the corporate responsibility for the ESD control measures at Infineon manufacturing sites worldwide. He is also involved in problem solving at customer production. Additionally, he provides the technical guidance for Infineon's corporate ESD device qualification and ESD system level testing. He is a member of the ESDA since 1990 being active in device testing standardization and in the TPC for many years. Since 1991 he is also an active member of the German ESD association (currently acting as Vice president). Since 1995 he represents Germany in the IEC standardization committee TC101 Electrostatics (as convenor of two working groups - static decay and device testing).

THURSDAY, NOVEMBER 8, 2012

Invited Talk 2: S20.20 Program Development

John Kinnear, IBM

This talk will provide an introduction to designing and implementing an ESD control program based on ANSI/ESD S20.20. John will discuss the tools and techniques of preparing for an ESD facility audit, the elements of an assessment, and the assessment process. The following topics will briefly be discussed: Administrative elements, ESD program assessment, ESD program techniques for different applications, Technical elements, the audit checklist and follow-up questions.

John Kinnear is an IBM Senior Engineer specializing in process & system technology, and facility certification in accordance with ANSI/ESD S20.20. He has a BS degree from University of Buffalo and a MS degree from Syracuse University. John has coordinated the testing of large mainframes for compliance to EMC, Safety, Environmental, Shipping and Volatile Organic Emission standards. He has also been the lead engineer on testing large mainframe systems to EMC emissions and immunity standards for FCC, CE Mark, VCCI and other national requirements. As a member of the ESD Association since 1990, John has served in several Standards Development Committees as well as association management positions. John is the appointed Technical Adviser to the United States National Committee/IEC Technical Committee 101, where he represents the United States to the International Electrotechnical Commission (IEC). As Chair of the ESDA's Facility Certification (ANSI/ESD S20.20) development program, John played major roles in the program's development and industry launch. In particular, John coordinated the initial development of Lead Assessor training, ISO Registrar Certification, and witness audits. John has served in every ESD Association officer's position, including Vice President, Senior Vice President and President. He is the past Chairman of the EOS/ESD Symposium Technical Program Committee and past General Chairman of the 2004 EOS/ESD Symposium.

TECHNICAL SESSIONS

WEDNESDAY, NOVEMBER 7, 2012

Technical Session 1A

1A.1: Issues & Solutions Involving Tape & Reel Induced ESD

Jane Pan, Donna Robinson, Fairchild Semiconductor

Presenting a study of ESD issues due to high charging but reportedly ESD safe tape and reel materials. This study includes both novel and industry standard testing of many types of tape and reel materials, a variety reported and potential issues due to the improper tape and reel materials, and proposed test standards to avoid these issues.

1A.2: Humidity Control Device for Static Charge Reduction

Albert Kow Kek Hing, ESD Consultancy, Sdn. Bhd.

This paper relates to a device comprising a moisture generation and delivery system to reduce or minimize static charges at any target area without the use of any air ionizer. Apart from keeping electrostatic voltages at safe levels, this device functions like a maintenance free ionizer hence realizing substantial cost savings

1A.3: S20.20 ESD Improvements for the Factory Floor

Richard Wong, Cisco Systems Inc.; Desmond Liu, 3M Corp.; Kum Weng Loo, Peter Gabrovsky, Xilinx Corp.

As component IO data rate increase, the component ESD protection is limited by the amount of capacitance that can be attached to IO. Thus, the handling of high speed components in the factory floor is becoming more critical. This paper will discuss factory floor issues that are not currently addressed by s20.20 but can lead to ESD handling issues.

1A.4: "Volume Conductive" Polyurethane and Epoxy Sealings and Thick Coatings Meet the Latest ESD Standards

Gerhard Kraus, StoCretec GmbH

Generally there are two ways to carry out an ESD flooring in an EPA. Depending on the requirements, floor coverings based on synthetic rubber or PVC as well as floor coatings based on epoxy or polyurethane resins are used. Since commercial carbon fiber loaded floor coatings often are having problems in meeting the latest ESD standards (e.g. Rtg via person/footwear/floor and walking test according to IEC 61340-5-1 [1] and ANSI/ESD S20.20-2007 [2]) their reputation is not the best. This paper gives information about the reasons, why common floor coatings have this non ideal behavior and provides solutions, achievable by applying advanced Epoxy- or Polyurethane sealings on top of the floor coatings or by using so called "volume conductive coatings" instead.

Technical Session 1B

1B.1: EOS Risk to Thin Oxides Contributed by Wrist-Strap Monitors

Scott Ward, Soo Leng Tan, Texas Instruments

Wrist straps have long been used to protect devices from electrostatic discharges (ESD). Constant monitoring wrist straps ensure, in real-time, that operators are properly grounded while handling devices. These same monitors, however, have been found to generate voltages at levels that put thin oxides at risk for EOS damage.

TECHNICAL SESSIONS

Technical Session 1B continued

1B.2: CDM Risk Mitigation with Air Ionization in Hi-Temp Automated Test Handler

Yohan Goh, Marcus Koh, Everfeed Technology Pte. Ltd.

Mass volume testing of semi-conductor devices using automated handling equipment (AHE) has prevailed for more than two decades. This has brought tremendous costs benefit; increase productivity and fast turn-around time for semi-conductor manufacturers. The underlying Charge Device Model (CDM) risks leading to catastrophic failure or latency issues with testing of Electrostatic Discharge Sensitive (ESDS) Devices in AHE, remain a well-known phenomenal widely reported by industry. Technology scaling and the ever-increasing demand on device operating speed pose a severe challenge to maintain the sensitivity of ESDS devices on-chip protection. There remain lots of existing and functional AHEs in semi-conductor manufacturers' test floor, built many years ago where there were little or no considerations on charge mitigation on testing of ESDS devices. This paper narrates fifty units of existing high temperature (Hi-Temp) AHE test handlers for high pin count ESDS Devices. The Hi-Temp AHE was designed and built more than 20-years ago, which remains functional but unable to meet new stringent AHE ESD customer specifications. The new AHE ESD requirements can be accomplished by understanding the need, customized design, installation and implementation with new novel concept in Hi-Temp air ionization and minimize risk of CDM whilst testing.

1B.3: Process ESD Compatibility Measurements

Arnold Steinman, Electronics Workshop and Dangelmayer Associates

There are no standards for establishing compatibility of a manufacturing process with the handling of devices of known ESD sensitivity. A prior paper established that voltages measured on components could correlate to device testing voltages. This paper makes measurements on different devices and people to compare with voltages and discharges of HBM and CDM testing.

Technical Session 1C

1C.1: Experiences with an Alternative Method for Grounding Personnel During Sitting Operation

CY Wong, CT Ong, KP Yan, Infineon Technologies

One of the major requirements for safe handling of IC´s is the grounding of personnel. The paper presents data about the effectiveness of using the floor/footwear system as primary means of grounding personnel in standing and sitting operation. It also discusses whether there is a contradiction with International Standards like IEC 61340-5-1 or ANSI/ESD S20.20.

1C.2: A Comparison of Electrostatic Discharge Models and Failure Signatures for Light-Emitting Diode

Gim Wae Goh, Osram Optos Semiconductor; Yohan Goh, Marcus Koh, Everfeed Technology Pte. Ltd.

ESD failures can occur in ESD protected areas in manufacturing environment that are well designed according to the latest ESD standards like ANSI S20.20 [1] or IEC 61340-5-1 [2]. The root cause for the failures can normally only be found by a detailed analysis of the whole production flow [3, 4].

1C.3: Implementing Air Ionizing Blower at KLA Tencor 2401 Metrology Tool Reduce Visual Inspection Failure for Semiconductor Wafers

Harriman Razman, Mohd Faizal Adris, Cha Tree Tow Woon, Silterra Malaysia Sdn. Bhd.

This paper describes the methodologies use for implementing effective air-ionizing blower at KLA Tencor 2410 (Viper) metrology tool for removing particles from outgoing wafers. After the implementation of this air-ionizing blower, achieved reduction of wafer lot failed visual inspection from 21.4% to 4.1% in Q2'2011.

THURSDAY, NOVEMBER 8, 2012

Technical Session 2A

2A.1: Investigating The Performance of Vacuum Formed Conductive and Dissipative trays Which are used for Handling and Storage of ESDS

Rainer Pfeifle, Wolfgang Warmbier GmbH & Co. KG

Vacuum formed trays are widely used in electronic production for handling and storage of ESD sensitive electronic circuits. Thee circuits are sensitive to electrostatic discharges and /or to electrostatic fields. ESDS in contact with surfaces shall dissipate their charge in a defined time to ground potential. While checking vacuum formed trays during ESD audits in many different locations, we have realized that a significant quantity of the trays when tested inside the cavities, do not comply with the standards recommendations regarding the safe handling of ESDS. This report shows test results of a vacuum formed tray that had been produced out of three different Polystyrene materials for a product qualification.

2A.2: ESD Levels and Trends for Advanced Memory Technologies

Yvonne Yeo Chii, Ang Ai Kiar, Jung Yoon, IBM

This paper presents a benchmarking study which was conducted to investigate the impact of aggressive technology scaling on the ESD levels of Advanced Memory Technologies. ESD qualification data were collected from various suppliers for DRAM and NAND Flash Memory technologies. The technology nodes range from 90nm down to 40nm for DRAMs and 60nm down to 25nm for Flash devices. The package types used were FBGAs for DRAMs and TSOP and LGAs for NAND Flash devices.

2A.3: Novel Strap to Achieve Less Than 50 Volt HBM on Normal Footwear

Albert Kow Kek Hing, ESD Consultancy, Sdn. Bhd.

HBM voltage control to a level of below 50 volts consistently has been difficult if not impossible in a manufacturing environment without wrist-strap in standing operations. By the addition of a stainless steel element into a custom designed foot grounder, a wearer can achieve typically less than 10 volts HBM consistently.

2A.4 Comparing Room Ionization Technologies in FPD Manufacturing

Joshua Yoo, Core Insight, Inc.; Dongsun Kim, JuYung Jeong, WonJoon Ho, LG Display Co., Ltd.; Arnold Steinman, Electronics Workshop

In FPD manufacturing, handling charges both sides of the glass panels. Ionizing bars over the top of the panels have a limited effect on ESD and particle contamination as the bottom of the glass remains charged. This paper examines charge generation in FPD manufacturing and proposes alternative ionization technology.

TECHNICAL SESSIONS

Technical Session 2B

2B.1: Reduction of Coupled Voltage of Electric Cable with Electro-Static Countermeasure

Takayoshi Ohtsu, Kentaro Hayashida, Yusaku Kobayashi, Shogo Imai, Shunsuke Okada, Suzuka National College of Technology; Yorioki Matsumoto, Matsumoto Giken Co. Ltd.

The failure by an electric noise caused by Electrostatic discharge (ESD) is one of the most important causes of reliability problems. It is important to reduce the fluctuation in a voltage of power supply for electric equipment. The metal covered cable is used to reduce an electric noise. It is effect on a shield of the electromagnetic wave because of the electric resistance on the surface of this cable is low. However, it is afraid of a fluctuation in a voltage due to the electrostatic discharge with the electric charged metal object. On the other hand, the insulation covered cable is used generally. It is afraid of a fluctuation in a voltage due to the electrostatic discharge by a tribo-charge. In this paper, the dissipative material covered cable was studied to reduce the fluctuation in a voltage.

2B.2: Compliance Verification of Static Dissipative Carrier for ESDS Devices in Semiconductor Backend Testing

Edmund Seah, Micron Semiconductor Asia Pte. Ltd.; Yohan Goh, Marcus Koh, Everfeed Technology Pte. Ltd.

In the semiconductor manufacturing testing environment, electrostatic sensitive (ESDS) semiconductor package is always being transported around in an electrostatic safe carrier. This is clearly stipulated in ANSI/ESD S20.20-2007 Section 8.3 “ESD protective packaging shall be in accordance with the contract, purchase order, drawing or other documentation”. This carrier will hold the ESDS package and transfer within Tri-Temp Test Handler(s) probes for testing before being removed from the carrier to the customer tray. These ESD safe carriers are usually made out of thermal plastic that has ability to withstand extreme temperature from -55 OC to 150OC. With these properties, Polyetherimide (PEI) and Polyethersulfone (PES) are most widely used.

2B.3: Evaluation of the Performance of Corona and Hybrid Alpha Ionizer Technology in Air and Nitrogen

Larry Levit, LBL Scientific; Geoff Weil, Anodyne Research

Ionizing pure Nitrogen is problematic, yet N2 applications are common. This study identified the charge carriers created by corona and hybrid Alpha ionizers and explained the voltage imbalances. It showed how to control them and make a stable N2 ionizer with hybrid Alpha technology. The positive charge carriers in N2 are N+ and the negative charges are free electrons with a small some Azide ions,_N_. Since electrons are 4 orders of magnitude lighter than that of Nitrogen atoms, the free electrons achieve much higher speeds than the ions and create a huge voltage imbalance when electrostatic forces drive the charge carriers. Voltage imbalance was measured for blower and bar type corona ionizers as well as for Alpha-based ionizers. The mechanisms for the imbalances are discussed. Extremely high voltages are required to create the free charges by corona and the same voltage is used to electrostatically propel the charge carriers away from the ionizer. In the case of Alpha source-based ionizers, the mechanism for liberating charge carriers is collisional and requires no high voltage. For a hybrid Alpha-electrical ionizer, there is no voltage threshold constraint for creating ions and a highly asymmetric voltage waveform is shown to deliver the charge carriers with excellent voltage balance. This cannot be achieved using the corona effect because the voltage threshold required to create ions, eliminates the option of asymmetric waveforms.

Technical Session 2C

2C.1: EMI-Caused EOS Exposure of Components and Its Mitigation

Vladimir Kraz, OnFILTER, Inc.

Increasing sensitivity of today’s components brings issue of electrical overstress (EOS) to the front, lines of efficient high-yield manufacturing. One of the main causes of EOS is electrical noise (EMI). This paper investigates the sources of EMI in electronic manufacturing and methods of mitigation of EOS exposure.

2C.2: HBM Concerns on Semiconductor Component (ICs) Mounted in Frame Form During Backend Manufacturing Processes

KK Ng, CY Wong, KP Yan, Infineon Technologies

At semiconductor backed manufacturing flow, before the “trim and form” process, IC components are mounted in frame form. Study had been carried out to determine the risk of ICs being damaged due to HBM ESD event through both grounded lead frame and (ungrounded) lead frame.

2C.3: ESD Control at Tape Drive and Tape Head Manufacturing

Johan Jr. Chan, Ruby Soliman, Michelle Lam, Rabic Hameed, IBM

ESD control program specifically designed for the ultra-sensitive magnetic tape head and drive manufacturing is described. The usage of a customized designed Discharge Event Audit (DEA) tool to implement ESD control is demonstrated. The importance of ESD control on the supplier side was also emphasized in the paper through DEA experiment demonstration.

2C.4: Minimizing Electrostatic Charge Generation and ESD Event in TFT-LCD Production Equipment

Dong-Sun Kim, Cun-bae Lim, Du-Seok Oh, Won-Joon Ho, Ju-Young Jeong, LG Display

In TFT LCD manufacturing processes, electrostatic charge generates when glass is separated from stages and its amplitudes closely related with vacuum pressure to holds the glass, holding times, separation cycles, lift pin height, lift speed and other various conditions throughout in the most TFT LCD processes. This paper examines how electrostatic generations are related between these factors. Also, glass lift pin materials should be insulators rather than static dissipative or conductive to protect ESD events. Residual charges on glass must be neutralize by ionizers to control ESD damage by separation from stage materials.

WORKSHOP

"Are we ready for 250 V CDM products?"

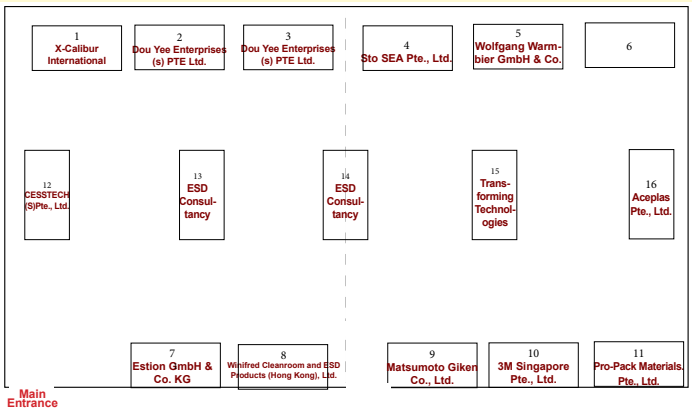
Moderator: Kep Pen Yan, Infineon Technologies Inc.

Email: Kep-Pen.Yan@infineon.com

The Industry Council on ESD Target Levels recommends a target level of 250V for the CDM robustness of semiconductor devices in their White Paper 2. This target is said to cover the economically achievable CDM robustness while it also guarantees a safe handling of devices in modern automated production lines. The workshop will address the actual status of CDM control measures in the factories and discuss whether this is enough for future more sensitive technologies. Another question is whether there is a need to develop new more advanced CDM control methods and how to implement them in the factories all over the world.

EXHIBITS

Promote your company by exhibiting at the EOS/ESD Symposium for Factory Issues. Table Top Exhibit Space Rental: $1,000.00 USD - payable to ESDA only. For more information visit http://esda.org/ESDSymposiumFactory.html



ALL BOOTH DIMENSIONS ARE THE SAME (6 FT TABLES)
Venue: TUV SUD PSB (Newton and Edison Rooms)

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